CMOS Processing Technology

Please send corrections (or suggestions) to youngwlim@hotmail.com.

This document was produced by using OpenOffice and Octave.

NAND Gate Layout View

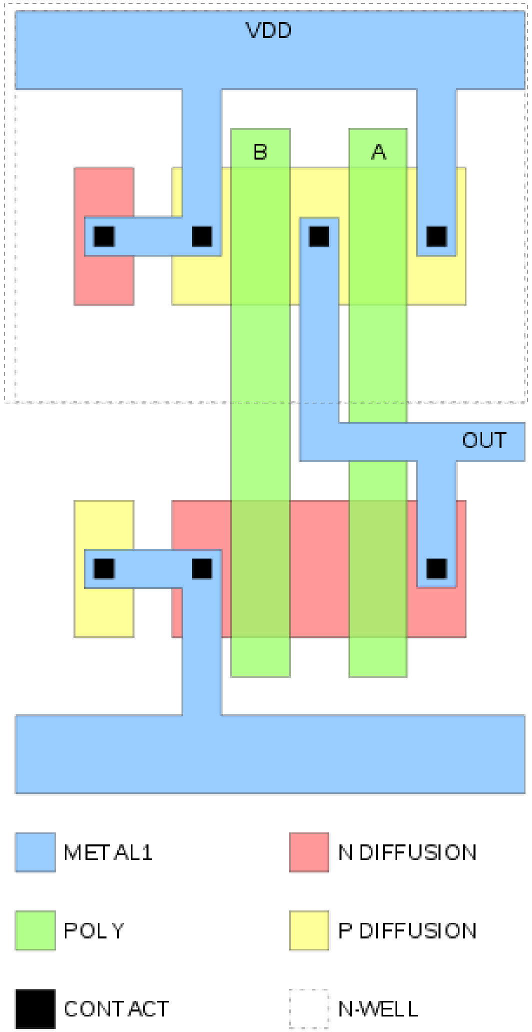
a "bird's eye view" of a stack of layers.
the circuit is constructed **on** a P-type substrate
the polysilicon, diffusion, and n-well : base layers - actually inserted into trenches of the P-type substrate
the contacts penetrate an insulating layer between the base layers and the first layer of metal (metal1)

The **inputs (A, B)** to the NAND (green) are in polysilicon.
The CMOS transistors are formed
by the intersection of the polysilicon and *diffusion*

- N diffusion for the N device (salmon)
- P diffusion for the P device (yellow)

the **output (out)** is connected together in metal (cyan)

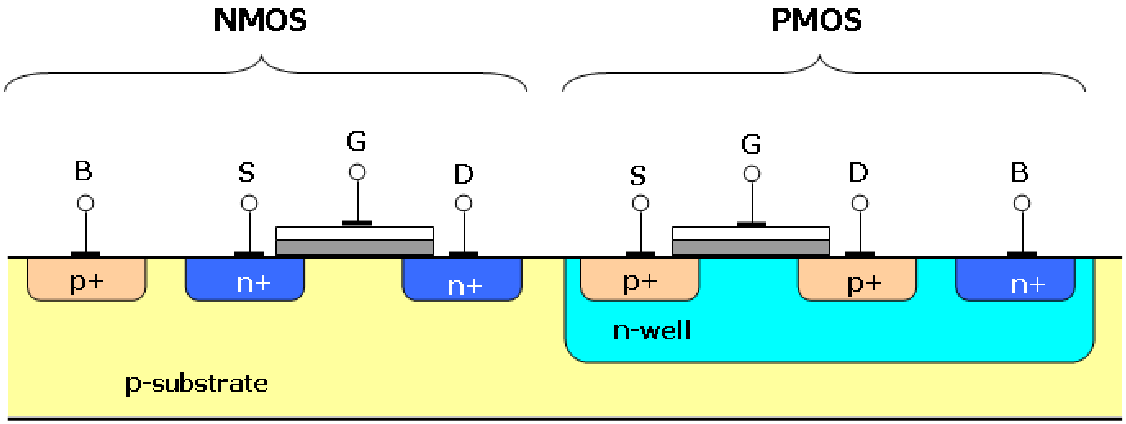
Connections between metal and polysilicon or *diffusion* are made through **contacts** (black)

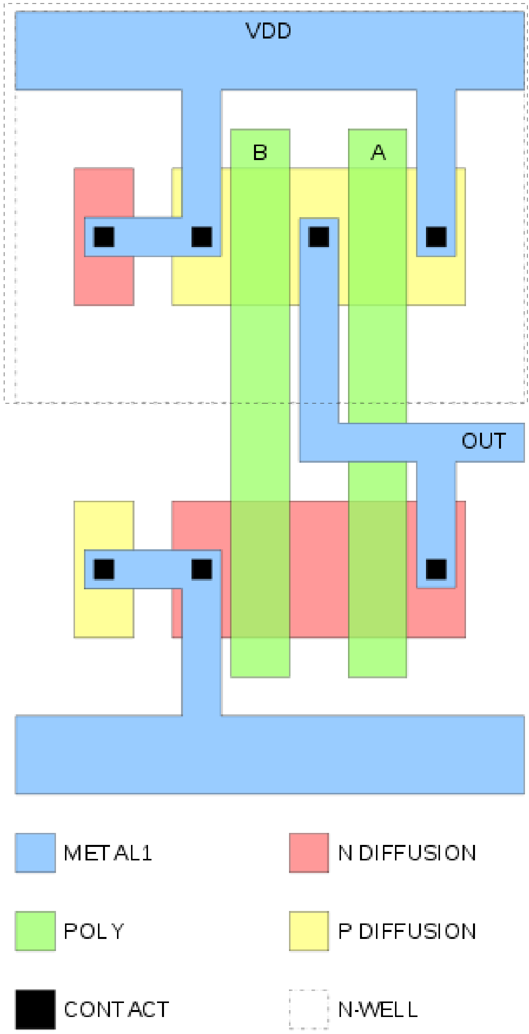


NAND Gate Cross Section View

the N device is manufactured on a P-type substrate
the P device is manufactured in an N-type well (n-well).

to prevent latchup
- a P-type substrate tap is connected to VSS
- an N-type n-well tap is connected to VDD





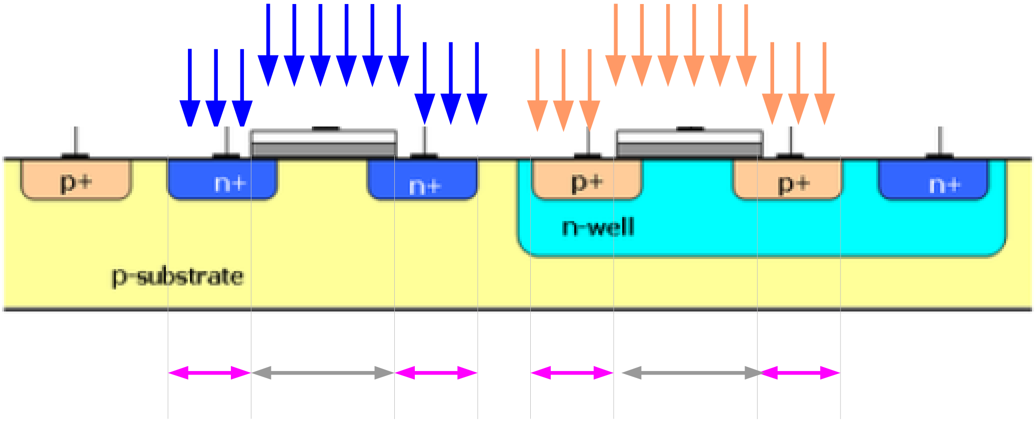
PolySilicon Gate Technology

self-aligned structure

the poly-silicon gate is used as a mask during the implantation

the source and drain regions are self-aligned with respect to the gate

- reduces the device size
- eliminates the large overlap capacitance between gate and drain
- maintains a continuous inversion layer between source and drain

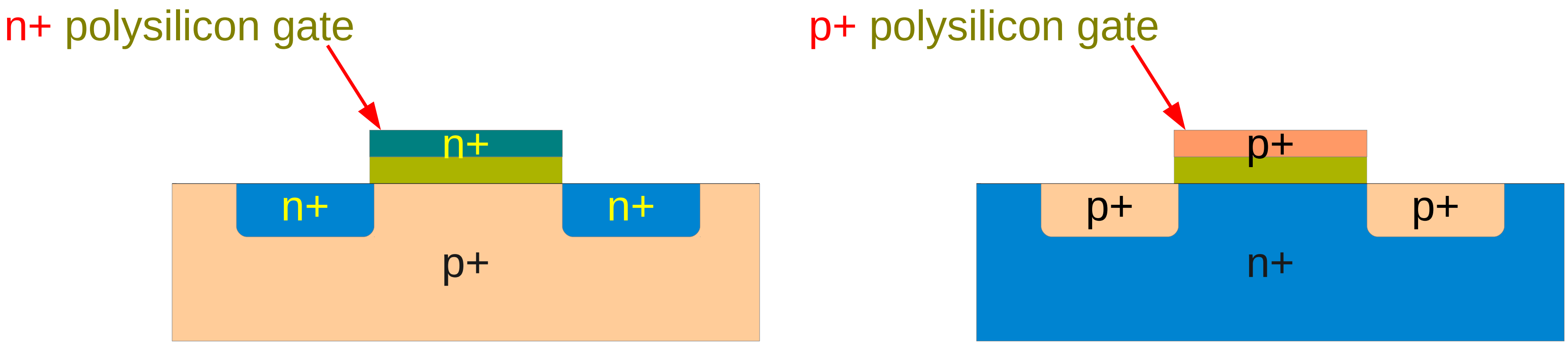


Dual-doped Polysilicon

But the conductivity of the poly-silicon layer is very low and
because of this low conductivity, the charge accumulation is low,
leading to a delay in channel formation and thus unwanted delays in circuits.

The poly layer is doped with N-type or P-type impurity
to make it behave like a perfect conductor and reduce the delay.

Polysilicon depletion effect is the phenomenon in which <u>unwanted variation</u> of threshold voltage of the MOSFET devices using polysilicon as gate material is observed, leading to unpredicted behaviour of the Electronic circuit.



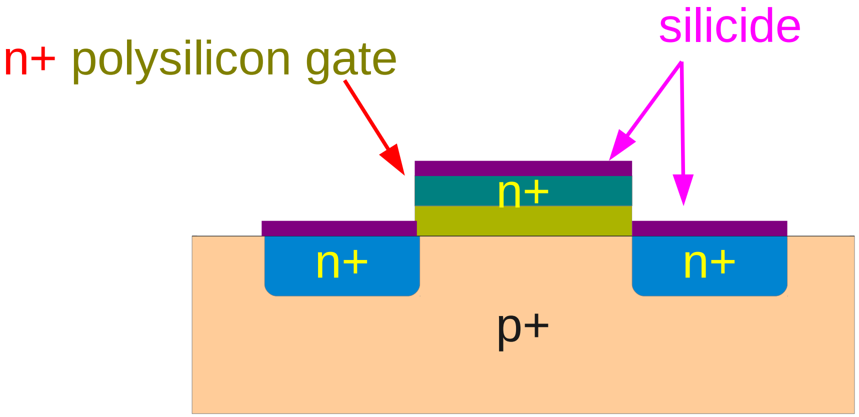
Polysilicon Wire

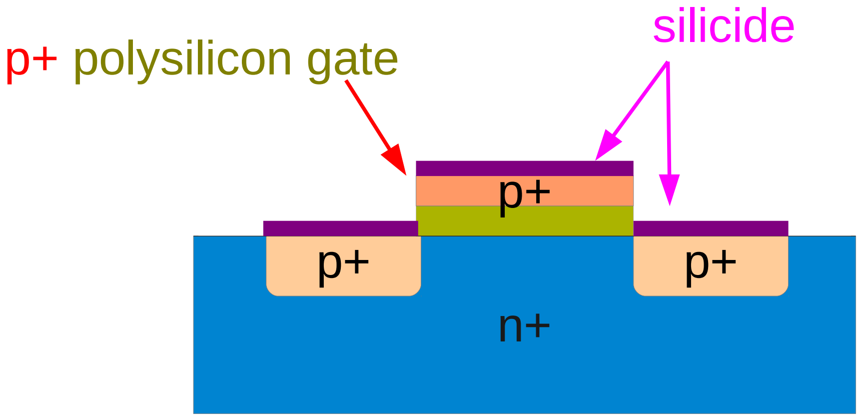
Poly is routed on top of FOX (Field Oxide)
FOX: the field that is not an active area and used for routing wires

Drawback of poly wire : high resistance ⇨ large delay
Metal: 0.1 ohm/square, Doped poly: 200 ohm/square

To reduce the resistance further, a **silicide** is deposited
over MOSFET (active) and FOX (field) regions

Silicide: a material that is a mixture of silicon a refractory metal like tungsten
Polycide: the silicide and poly gate sandwich





PolySilicon Depletion Effect (1)

The gate contact may be of polysilicon or metal,
previously polysilicon was chosen over metal
because the interfacing between polysilicon and gate oxide (SiO2) was favourable.

Polysilicon depletion effect is the phenomenon in which unwanted variation of threshold voltage of the MOSFET devices using polysilicon as gate material is observed, leading to unpredicted behaviour of the Electronic circuit.

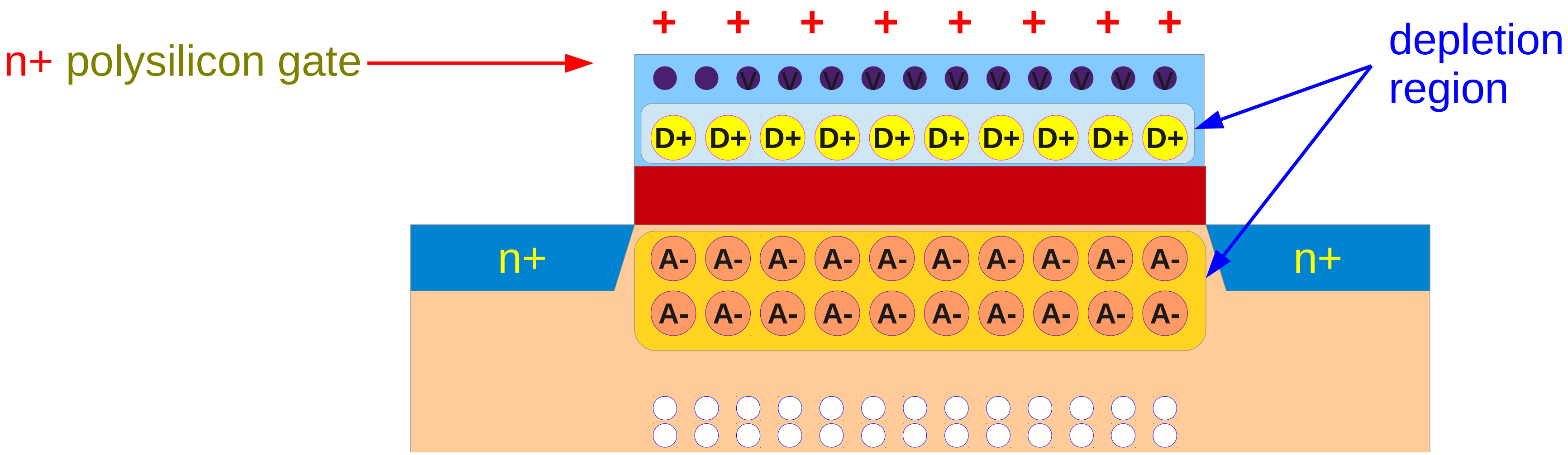
The effect with doped poly is an undesired reduction of threshold voltage that wasn't taken into account during circuit simulation. In order to avoid this kind of variation in vth of the MOSFET, at present metal gate is preferred over polysilicon.

High-k Dielectric Metal Gate (HKMG)
Metal gates were re-introduced at the time when SiO2 dielectrics are being replaced by high-k dielectrics like Hafnium oxide as gate oxide in the mainstream CMOS technology.

PolySilicon Depletion Effect (2)

When a positive field is applied on the gate, the scattered carriers arrange
the electrons move closer toward the gate terminal
but due to the open circuit configuration they don't start to flow.
As a result a depletion region is formed on the polysilicon-oxide interface

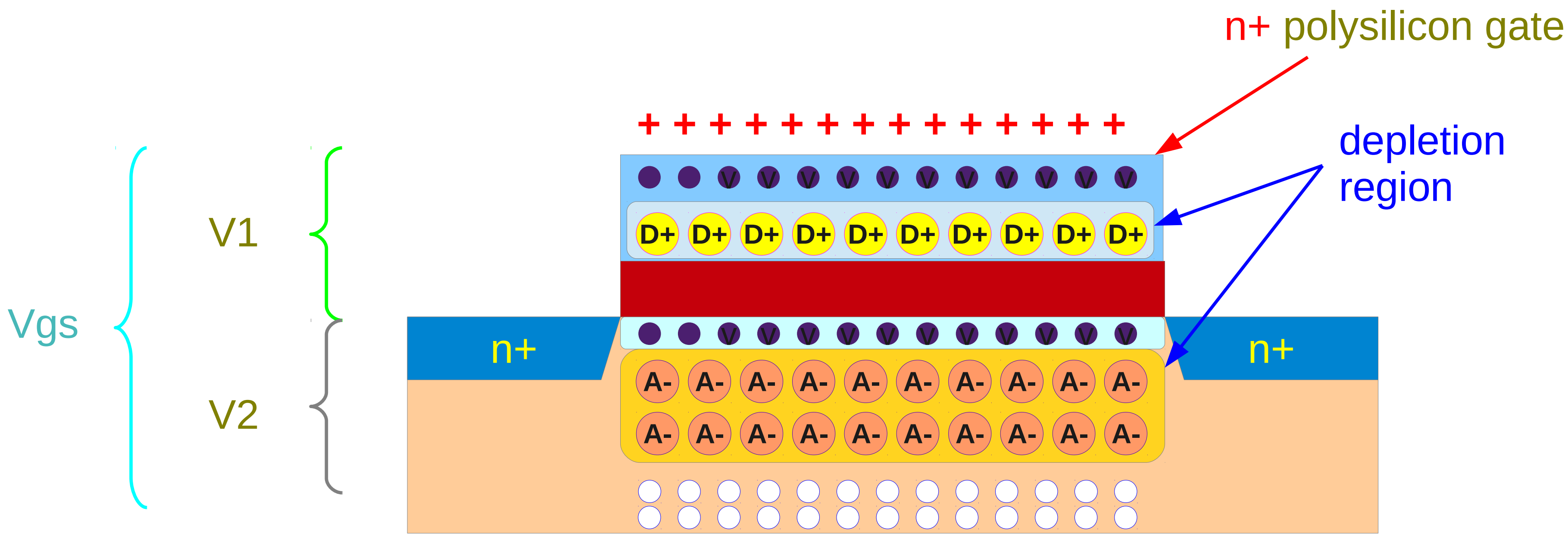
In an NMOS with n+ polysilicon gate,
the **poly depletion effect** helps the channel formation
by the combined effect of the (+)ve field of donor ions (ND)
and the externally applied (+)ve field at gate terminal.



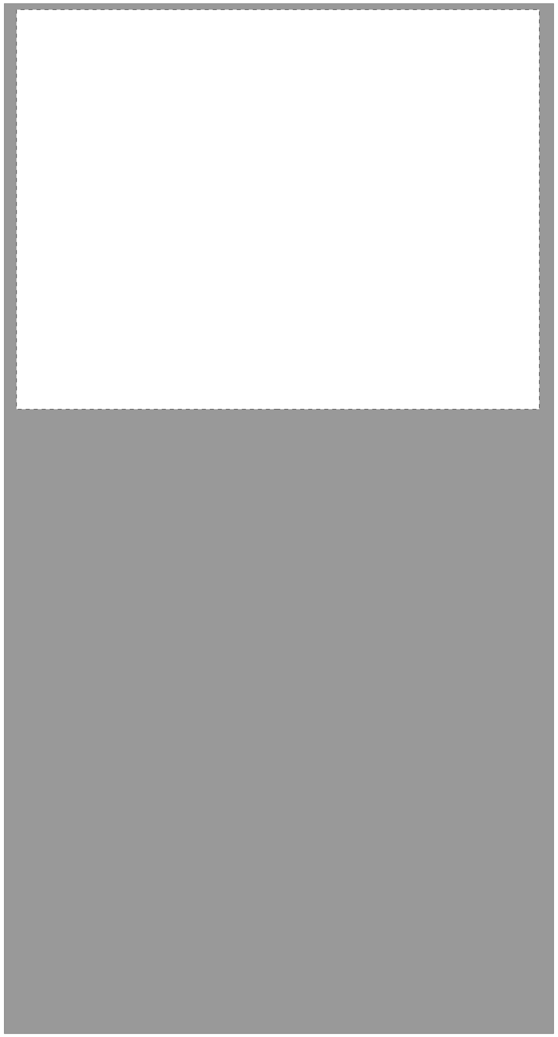
PolySilicon Depletion Effect (3)

Basically the accumulation of the (+)ve charged donor ions (ND) on the polysilicon **enhances** the formation of the inversion channel and
when Vgs > Vth an inversion layer is formed,

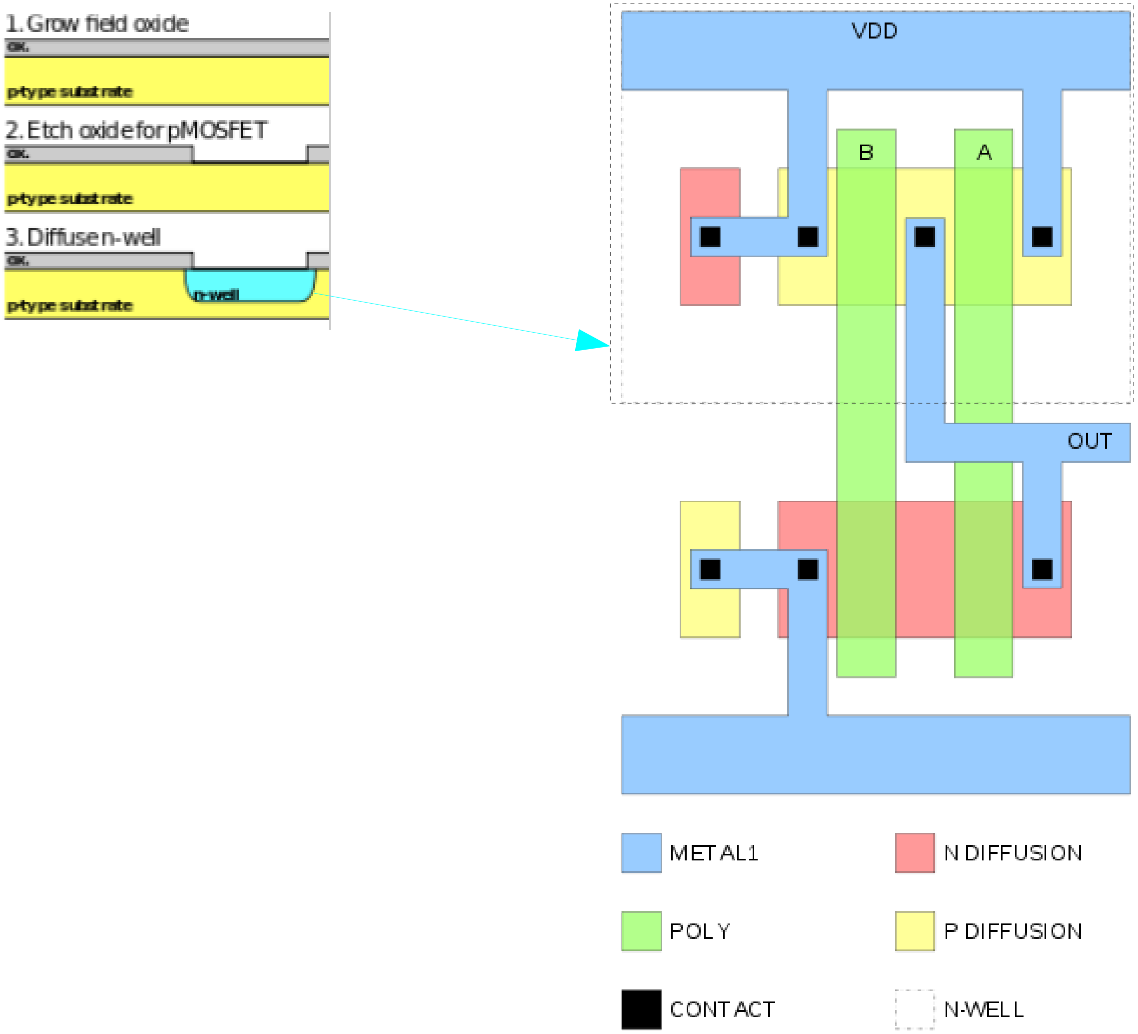
undesired reduction of threshold voltage



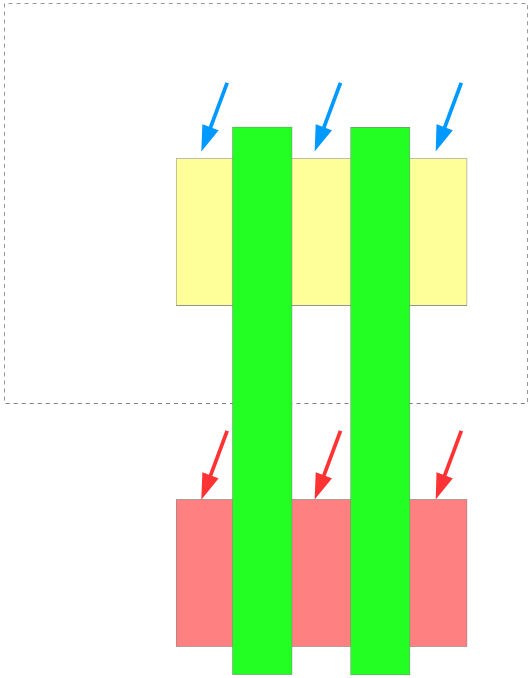
N-well

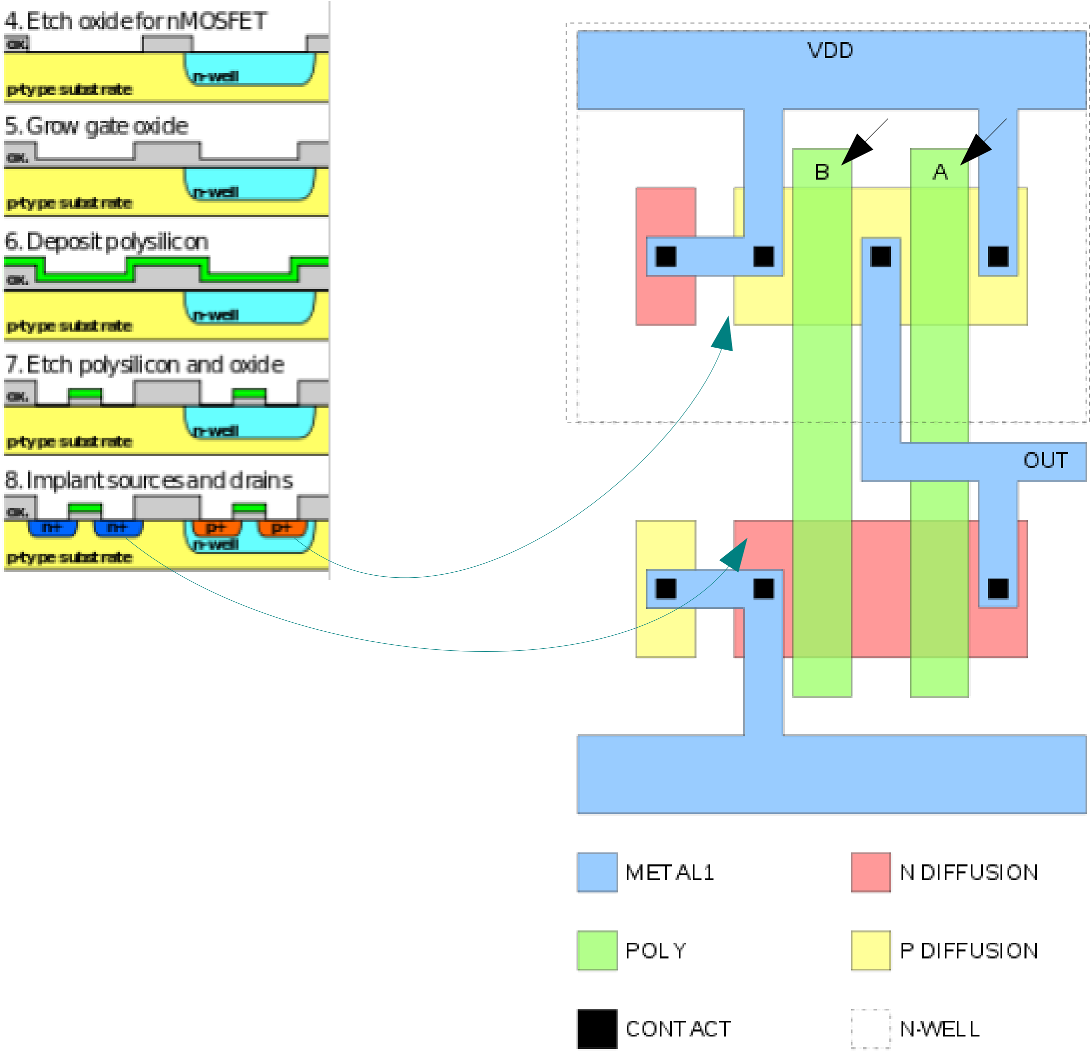


N-well mask

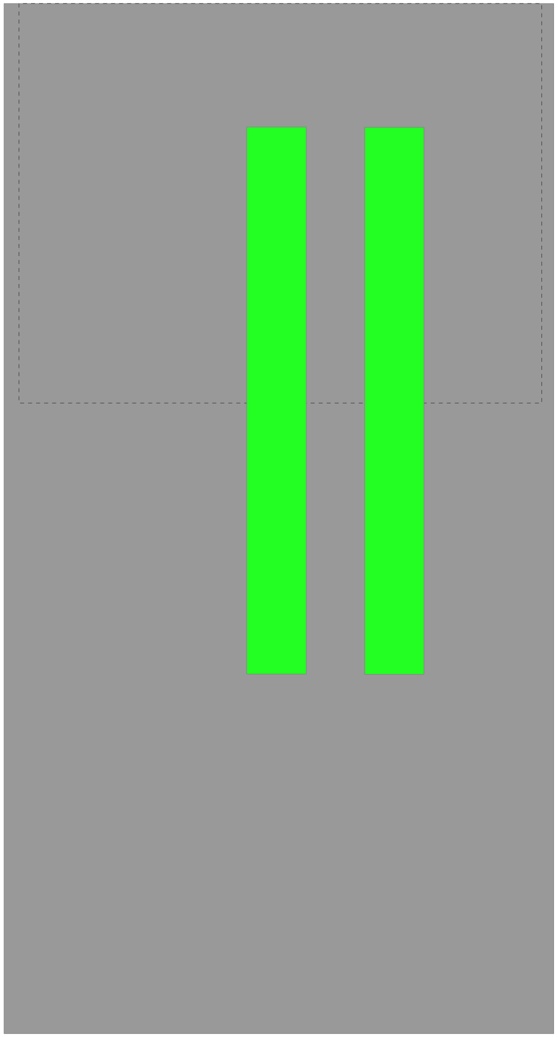


Diffusion

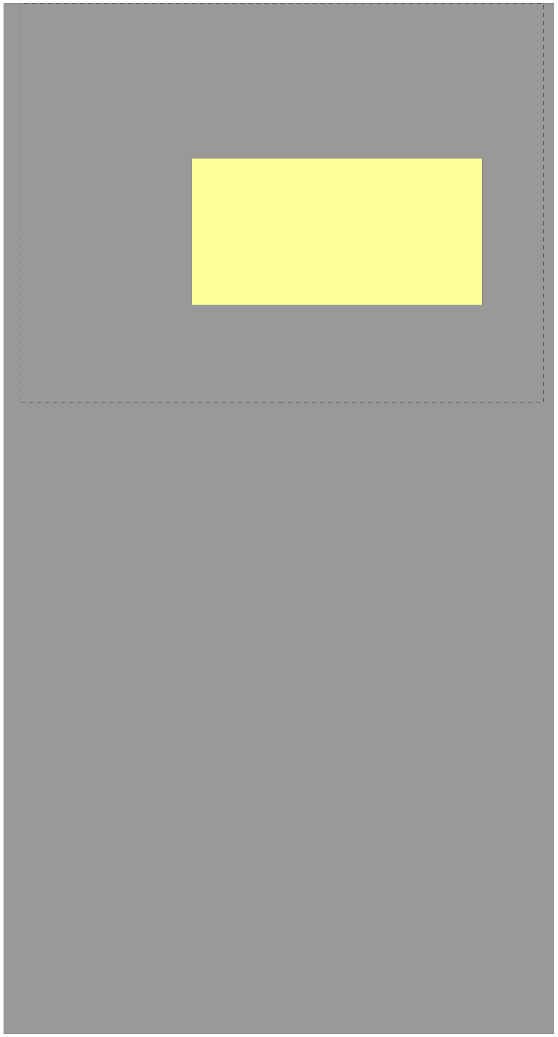



4. Etch oxide for nMOSFET
ox.
p-type substrate
n-well
5. Grow gate oxide
6. Deposit polysilicon
7. Etch polysilicon and oxide
8. Implant sources and drains
n+
p+
VDD
B
A
OUT
METAL1
N DIFFUSION
POLY
P DIFFUSION
CONTACT
N-WELL

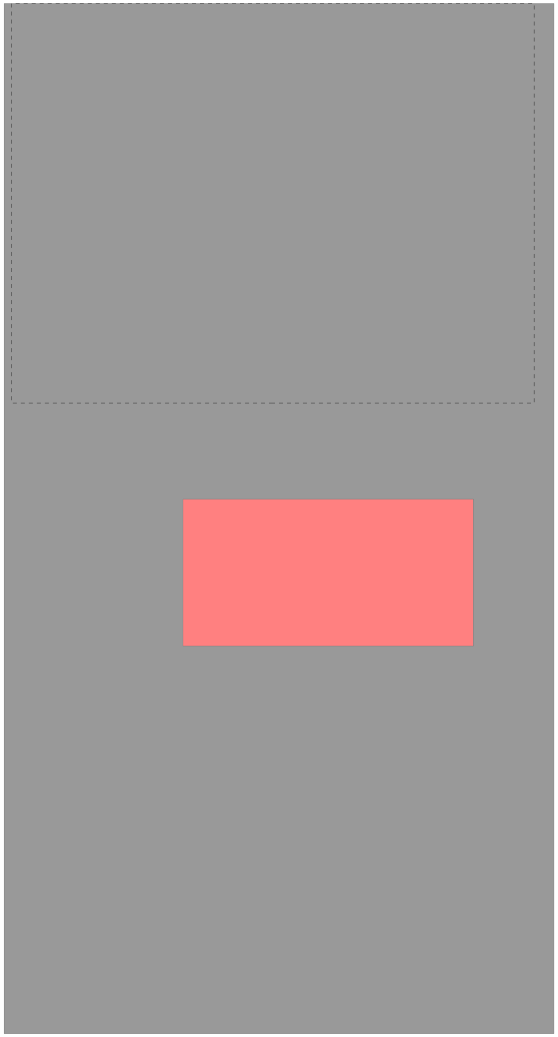
Diffusion Masks



Polysilicon mask

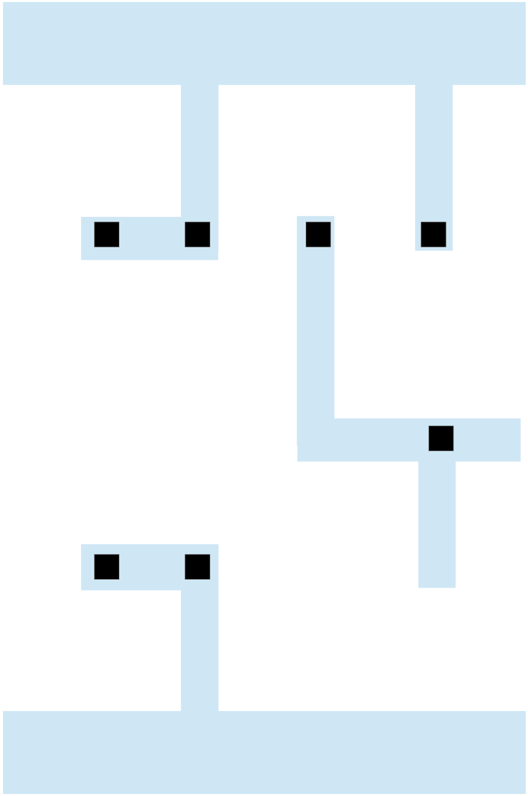


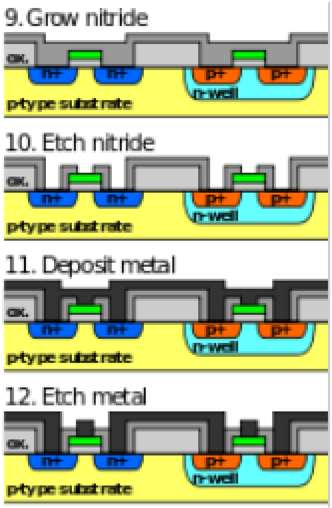
n+ mask

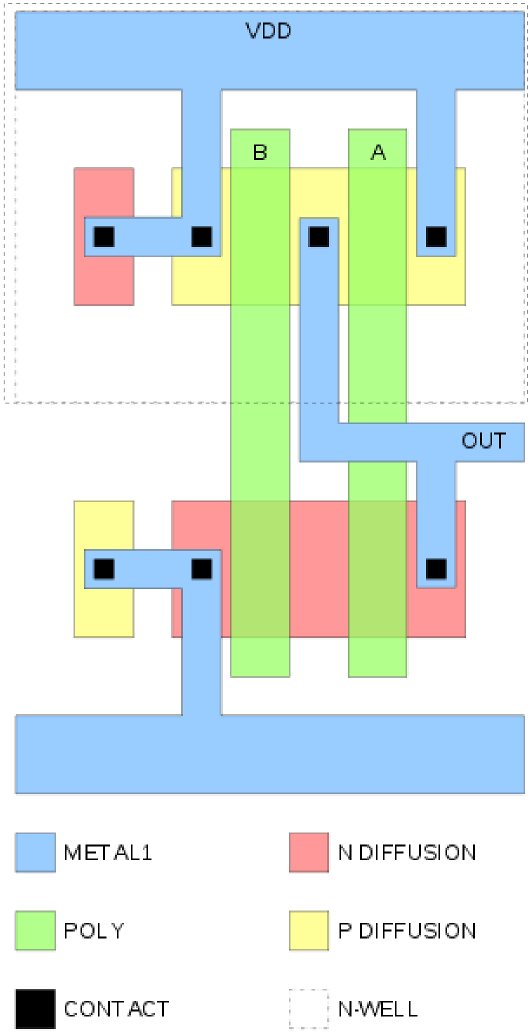


p+ mask

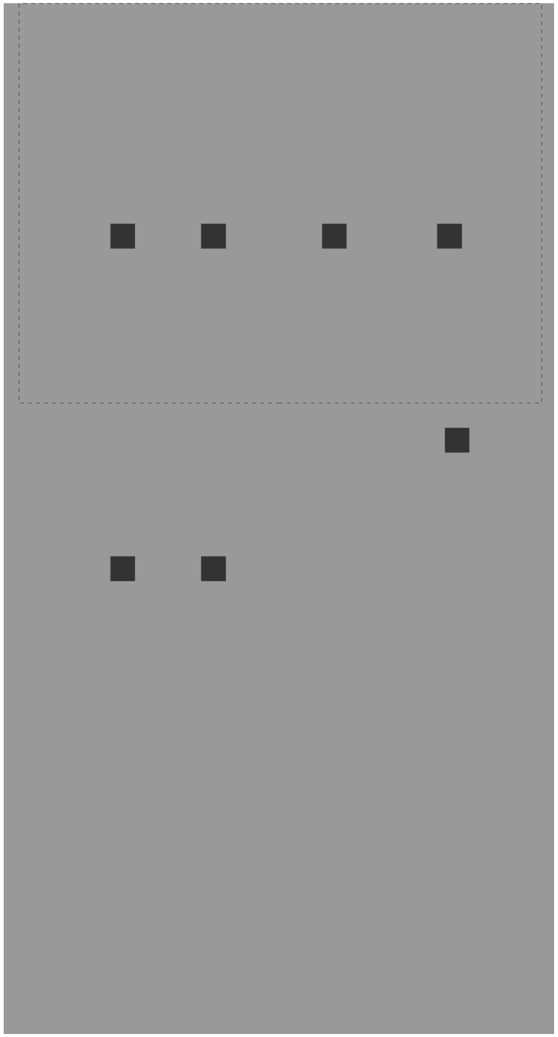
Metallization



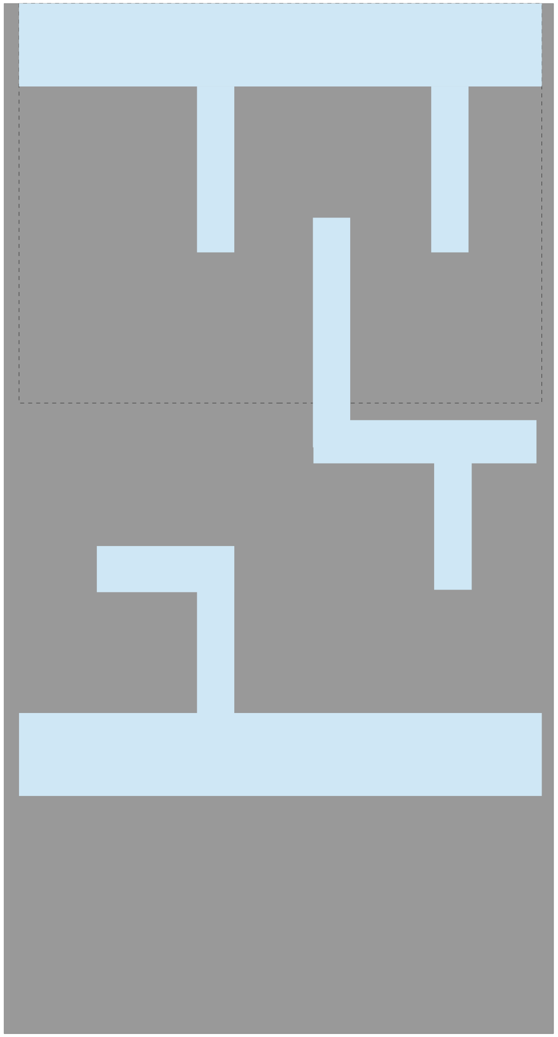




Metallization Masks



Contact mask



Metal mask

Dielectric

References

[1] http://en.wikipedia.org/